

FIELD EFFECT TRANSISTOR STRUCTURE WITH ABRUPT SOURCE/DRAIN JUNCTIONS

Background of the Invention

Field of the Invention

The invention relates to metal-oxide-semiconductor field effect transistors (MOSFETs) and more particularly to transistor structures having abrupt junctions, and methods of making same.

Background

The trend of integrating more functions on a single substrate while operating at ever higher frequencies has existed in the semiconductor industry for many years. Advances in both semiconductor process technology and digital system architecture have aided in producing these more highly integrated and faster operating integrated circuits.

The desired result of many recent advances in semiconductor process technology has been to reduce the dimensions of the transistors used to form the individual circuits found on integrated circuits. There are several well-recognized benefits of reducing the size of transistors. In the case of MOSFETs, reducing the channel length provides the capability to deliver a given amount of drive current with a smaller channel width. By reducing the width and length of a FET, the parasitic gate capacitance, which is a function of the area defined by the width and length can be reduced, thereby improving circuit performance. Similarly, reducing the size of transistors is beneficial in that less area is consumed for a given circuit, and this allows more circuits in a given area, or a smaller, less costly chip, or both.

It has also been well known that MOSFETs can not simply be scaled down linearly. That is, as the width and length attributes of a MOSFET are reduced, other parts of the transistor, such as the gate dielectric and the junctions must also be scaled so as to achieve the desired electrical characteristics. Undesirable electrical characteristics in MOSFETs due to improper scaling include coupling of the electric field into the channel region and increased subthreshold conduction. These effects are sometimes referred to in this field as short channel effects.

A number of methods have been developed to form ever more shallow source/drain junctions for MOSFETs in order to achieve proper scaling. Unfortunately, these very shallow junctions create source/drain extensions that have increased resistivity as compared with deeper source/drain junctions. In longer channel length MOSFETs with deeper source/drain junctions, the source/drain extension resistivity was negligible compared to the on-resistance of the MOSFET itself. However, as MOSFET channel lengths decrease into the deep sub-micron region, the increased source/drain extension resistivity becomes a significant performance limitation.

What is needed is a field effect transistor structure having very short channel length and low source/drain extension resistivity, yet operable to produce high drive currents without suffering from the short channel effects that produce significant levels of off-state current. What is further needed is a method of manufacturing such a structure.

Summary of the Invention

Briefly, a MOSFET structure includes highly conductive source/drain extensions of a first conductivity type, and super abrupt junctions with a semiconductor body of a second conductivity type.

In a further aspect of the invention, a process for forming a MOSFET includes removing portions of the substrate to form recesses that are adjacent and partially subjacent a FET gate structure, and back filling the recesses with an epitaxial process.

Brief Description of the Drawings

Fig. 1 is a schematic cross-section of a wafer in process showing a substrate with a gate dielectric formed thereon, and a patterned gate electrode over the gate dielectric and a spacer layer formed over the surface of the wafer.

Fig. 2 is a schematic cross-section showing the structure of Fig. 1, after an anisotropic etch of the spacer layer forms thin sidewall spacers, and the gate dielectric not covered by the gate electrode or sidewall spacers is removed.

Fig. 3 is a schematic cross-section showing the structure of Fig. 2, after an isotropic etch removes portions of the substrate, to form recesses therein, and further showing a portion of the gate electrode etched away.

Fig. 4 is a schematic cross-section showing the structure of Fig. 3, after the recesses have been back-filled and the gate electrode thickness built up.

Fig. 5 is a schematic cross-section showing the structure of Fig. 4, after a salicidation operation.

Fig. 6 is a schematic cross-section showing the structure of Fig. 3, after an alternative process flow in which the back-filling of the recesses includes forming a layer of a first conductivity type followed by formation of a layer of a second conductivity type.

Fig. 7 is a flow diagram illustrating the various operations in a manufacturing process in accordance with the present invention.

Detailed Description

Overview

Conventional source/drain junction formation is accomplished by an ion implantation operation that is self-aligned to the gate electrode, or alternatively, aligned to sidewall spacers that are adjacent to the gate electrode. Reasonable transistor performance has been achieved in this way for many generations of semiconductor process technology. However, as transistor scaling has brought FET channel lengths down into the deep sub-micron region, the changes to source/drain junction depth and doping concentration required to achieve desirable electrical performance of FETs have increased the parasitic resistance associated with the FET source/drain terminals to the point where this parasitic resistance is significant compared to the on-resistance of the FET. In this field, the parasitic resistance is sometimes referred to as external resistance. More particularly, simultaneously obtaining the very shallow junction depth, high source-drain extension doping concentration, and abrupt change in doping profile between the body and source/drain junctions, all required for desirable electrical performance in deep submicron FETs has become extremely difficult to achieve with conventional processes.

An illustrative embodiment of the present invention provides a FET with highly conductive source/drain extensions and abrupt junctions. Methods of forming the FET structure of the present invention include isotropically etching the substrate adjacent to, and partially underneath, the gate dielectric layer of a FET, and selectively depositing bilayers of in-situ doped material of a first conductivity type, and a second conductivity type.

FETs embodying the present invention include back-filled source and drain terminals. In this way, the doping concentration of the source/drain terminals can be controlled by controlling the gas mixture, temperature, and pressure, in a reaction chamber. With the precise control of doping concentration of the material being deposited, the embodiments of the present invention include microelectronic devices having very abrupt junctions. Furthermore, particular embodiments of the present invention may eliminate high-energy ion implantation of the source/drain junctions. Formation of the source/drain junctions in this way also provides increased margin for the process thermal budget, since a high temperature operation is not required to activate the dopants, or to thermally in-diffuse the dopants into the tip portion of the source/drain terminals.

Terminology

The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

The terms metal line, trace, wire, conductor, signal path and signaling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnect or simply metal. Metal lines, generally aluminum (Al), copper (Cu) or an alloy of Al and Cu, are conductors that provide signal paths for coupling or interconnecting, electrical circuitry. Conductors other than metal are available in microelectronic devices. Materials such as doped polysilicon, doped single-crystal silicon (often referred to simply as diffusion,

regardless of whether such doping is achieved by thermal diffusion or ion implantation), titanium (Ti), molybdenum (Mo), cobalt (Co), nickel (Ni) and tungsten (W) and refractory metal silicides are examples of other conductors.

The terms contact and via, both refer to structures for electrical connection of conductors from different interconnect levels. These terms are sometimes used in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure contact and via refer to the completed structure.

Epitaxial layer refers to a layer of single crystal semiconductor material.

The term "gate" is context sensitive and can be used in two ways when describing integrated circuits. As used herein, gate refers to the insulated gate terminal of a three terminal FET when used in the context of transistor circuit configuration, and refers to a circuit for realizing an arbitrary logical function when used in the context of a logic gate. A FET can be viewed as a four terminal device when the semiconductor body is considered.

Polycrystalline silicon is a nonporous form of silicon made up of randomly oriented crystallites or domains. Polycrystalline silicon is often formed by chemical vapor deposition from a silicon source gas or other methods and has a structure that contains large-angle grain boundaries, twin boundaries, or both. Polycrystalline silicon is often referred to in this field as polysilicon, or sometimes more simply as poly.

Source/drain terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of an electric field resulting from a voltage applied to the gate terminal. Source/drain terminals are typically formed in a semiconductor substrate and have a conductivity type (i.e., p-type or n-type) that is the opposite of the conductivity type of the substrate. Sometimes, source/drain terminals are referred to as junctions. Generally, the source and drain terminals are fabricated such that they are geometrically symmetrical. Source/drain terminals may include extensions, sometimes referred to as tips, which are shallower than other portions of the source/drain terminals. The tips typically extend toward the channel region of a FET, from

the main portion of the source/drain terminal. With geometrically symmetrical source and drain terminals it is common to simply refer to these terminals as source/drain terminals, and this nomenclature is used herein. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the FET is operated in a circuit.

Substrate, as used herein, refers to the physical object that is the basic workpiece that is transformed by various process operations into the desired microelectronic configuration. A substrate may also be referred to as a wafer. Wafers, may be made of semiconducting, non-semiconducting, or combinations of semiconducting and non-semiconducting materials.

The term vertical, as used herein, means substantially perpendicular to the surface of a substrate.

Referring to Figs. 1-6, an illustrative embodiment of the present invention is described. As shown in Fig. 1, a wafer is processed in known ways to form a thin film layer over a patterned gate electrode and over a gate dielectric layer that has been disposed on the top surface of the wafer. More particularly, as shown in Fig. 1, a substrate **102** has a gate dielectric layer **104** disposed over the surface thereof, and a patterned gate electrode **106** is formed over gate dielectric layer **104**. In the illustrative embodiment, substrate **102** is a silicon wafer, gate dielectric layer **104** is a silicon dioxide layer, and gate electrode **106** is formed from polysilicon. Although gate dielectric layer **104** is typically a thin layer of oxidized silicon, the thickness and chemical make-up of the gate insulator layer may be varied within the scope of the invention.

Those skilled in the art and having the benefit of this disclosure will recognize that although field oxide regions are not shown in the Figures, the operations and structures shown and described herein, are compatible with various field oxide isolation architectures. Examples of field oxide isolation architectures include shallow trench isolation regions in a surface of a substrate, and the older local oxidation of silicon, which formed non-planarized oxide isolation regions.

A thin film layer 108 is deposited over the surface of gate electrode 106 and the portions of gate dielectric layer 104 not already covered by gate electrode 106. Thin film layer 108 may also be referred to as a spacer layer because spacers adjacent to the side walls of gate electrode 106 are formed from layer 108 in subsequent processing operations. It is preferable for spacer layer 108 to have etch characteristics that are different from the etch characteristics of substrate 102 and gate electrode 106. The material for spacer layer 108 could be any dielectric material including, but not limited to, nitride, oxynitride, and oxide. In the illustrative embodiment, subsequent to the polysilicon etch that forms gate electrode 106, a thin layer of silicon nitride is deposited over the surface of the substrate to form spacer layer 108. In one embodiment, the silicon nitride layer is approximately 20 nm thick, and is formed in a vertical diffusion furnace. However, the thickness of the nitride layer is not a limitation of the invention and it may be made any practical thickness, for example, in a range of from 2 nm to 50 nm thick. This nitride layer will be used to provide the needed selectivity during a subsequent epitaxial backfill operation. Similarly, the spacer layer may be formed of another material such as, for example, silicon dioxide. Silicon dioxide has a dielectric constant that is lower than the dielectric constant of silicon nitride, and this is advantageous in terms of lowering parasitic capacitance between the gate electrode and other nearby circuit nodes.

Referring to Fig. 2, spacer layer 108 is etched anisotropically using, for example, conventional dry etch chemistries for silicon nitride. Subsequent to this etch operation, no significant amount of residual silicon nitride remains in the source/drain regions. In the illustrative embodiment, this anisotropic etch operation leaves a nitride layer approximately 150nm thick (when measured along a vertical axis) along the sidewalls of polysilicon gate electrode 106. Typically, the vertical height (i.e., thickness) of this layer is approximately equal to the thickness of gate electrode 106. These post-etch nitride structures are referred to as spacers. As can be seen in Figs. 1-2, that portion of silicon nitride spacer layer 108 that is superjacent to the top surface of gate electrode 106 is removed by the spacer layer etch operation.

Referring to Fig. 3, a plurality of recesses in substrate 102 are produced by using an isotropic dry etch process in a parallel plate RF plasma etching system. A mixture of sulfur

hexafluoride (SF_6) and helium (He), at process conditions that favor isotropy are employed. Such conditions include high pressure and low RF power density. In one embodiment of the present invention, a process pressure of approximately 900 mT, a gap of 1.1 cm, an RF power of 100 W, a He flow of 150 sccm, and a SF_6 flow of 100 sccm is used. RF power may be varied in a range, for example, of 50 W to 200 W, and the process pressure may be varied but should be greater than approximately 500 mT. This etch process is highly selective and is characterized by a silicon etch rate that is much greater than the etch rate of the silicon dioxide that forms gate dielectric layer **104**. Similarly, the etch rate of silicon substrate **102** is much greater than the etch rate of the silicon nitride that forms sidewall spacers **108**. The electrical characteristics of gate dielectric layer **104** are not adversely affected by the etch process that forms the recesses in substrate **102**.

As can be seen in Fig. 3, the recesses include a portion that underlies gate dielectric layer **104**. In the illustrative embodiment, substrate **102** is etched isotropically such that the lateral etch creates a recessed area that reaches underneath not only the spacer but also partially underneath a region defined by overlying gate electrode **106**.

Note that, since silicon nitride spacer layer **108** was removed from the top surface of polysilicon gate electrode **106**, the etch that forms the recess also etches the top surface of polysilicon gate electrode **106**, thereby reducing its height as shown in Fig. 3.

Those skilled in the art and having the benefit of this disclosure will recognize that the operations and structures disclosed above are applicable to the formation of both n-channel FETs (NFETs) and p-channel FETs (PFETs). PFETs and NFETs are structurally similar, however the relative placement of p-type and n-type dopants is different. That is, a PFET includes p-type source/drain terminals in an n-type body, and an NFET includes n-type source/drain terminals in a p-type body.

The illustrative embodiment is described in terms of the formation of a PFET. It should be recognized that the present invention applies to the structure and manufacture of NFETs as well. Referring now to Fig. 4, an epitaxial film of boron doped Si **110** is formed using SiH_2Cl_2 ,

based chemistry such that the deposition is highly selective to nitride spacer 108, i.e., the film of boron doped Si 110 does not form on, nor adhere to, silicon nitride spacer 108. However, the recesses are substantially filled by this deposition operation. The recess may be completely filled by this operation. No ex-situ cleaning operations are performed. This is because an external wet clean would tend to damage thin gate dielectric layer 104. In an alternative embodiment, boron doped SiGe may be used in place of boron doped Si to form the film that fills the recess.

Typically, epitaxial film 110 is deposited such that its top surface is above the plane of the original surface of substrate 102. This can be seen in Fig. 4 by comparing the relative positions of gate dielectric layer 104, which was formed on the original surface of substrate 102, with the top surface of Si layer 110. As is further shown in Fig. 4, an epitaxial film of boron doped Si 110 is also formed on top of gate electrode 106. In this way the thickness of polysilicon gate electrode 106 is increased from its post-etch dimensions.

Still referring to Fig. 4, boron doped Si film 110 is formed by a selective deposition. A selective deposition of silicon, or a silicon alloy such as silicon germanium, forms silicon, or the silicon alloy, on the exposed silicon surfaces. For example, a selective deposition of boron doped silicon creates Si film 110 on the exposed surfaces of silicon substrate 102, and polysilicon gate electrode 106. A silicon film can be selectively deposited by heating the wafer to a temperature of approximately 600 °C to 900 °C, providing a deposition gas comprising dichlorosilane (SiH_2Cl_2), and hydrogen (H_2). More particularly, an n-type silicon can be selectively deposited at a temperature of approximately 750°C, with approximately 10 slm H_2 , approximately 30 sccm HCl , approximately 100 sccm SiH_2Cl_2 , and approximately 180 sccm PH_3 , at approximately atmospheric pressure. Such process conditions can deposit a layer approximately 50 nm thick in approximately 6 minutes. A p-type silicon can be selectively deposited at a temperature of approximately 800°C, with approximately 20 slm H_2 , approximately 70 sccm HCl , approximately 120 sccm SiH_2Cl_2 , and approximately 75 sccm B_2H_6 . Such process conditions can deposit a layer approximately 50 nm thick in approximately 155 seconds.

A silicon germanium alloy can be selectively deposited by heating the wafer to a temperature between approximately 700 °C and 750 °C, providing a deposition gas mix comprising dichlorosilane at a rate of between approximately 10 to 100 sccm, 1% hydrogen diluted germane (GeH_4) at a rate of between approximately 10 to 200 sccm, and hydrogen at a rate of approximately 20 slm into a CVD chamber maintained at a pressure between approximately 50 to 760 torr. A dopant gas such as diborane, phosphine, or arsine, can be included in the process gas mix if a doped silicon or silicon alloy film is desired.

A highly doped ($>5 \times 10^{20}$ atoms/cm³) n-type silicon germanium epitaxial film can be selectively deposited onto silicon surfaces by thermal chemical vapor deposition utilizing a deposition gas mix comprising approximately 10 to 200 sccm GeH_4 , approximately 10 to 100 sccm dichlorosilane, 10 to 40 slm H_2 , 1 to 200 sccm PH_3 , and 15 sccm HCl , while maintaining the substrate at a temperature between 700°C and 750 °C and maintaining a deposition pressure of approximately 165 torr during film deposition. Such a process will form a substantially uniformly doped n-type silicon germanium epitaxial film. Similarly, a p-type silicon germanium alloy can be formed by decomposition of approximately 20 sccm of dichlorosilane, approximately 80 sccm germane, approximately 20 slm H_2 and a p-type dopant source, such as approximately 1 -200 sccm of B_2H_6 at a temperature of approximately 740°C. In order to increase the selectivity of the deposition process, approximately 10 sccm of HCl can be added to the gas mix. Such process conditions can deposit a layer approximately 50 nm thick in approximately 75 seconds.

Those skilled in the art and having the benefit of this disclosure, will recognize that, the deposition operation is such that selectivity to oxide in field oxide regions, or shallow trench isolation regions is also achieved.

Fig. 5 shows the FET structure of Fig. 4 after further processing operations are performed. Conventional processing may be used to form additional sidewall spacers 112 that are disposed along opposing sidewall spacers 108. Furthermore, conventional processing may be used to form salicided regions 114 over the top surfaces of doped Si regions 110, that is, the

source/drain extension regions and polysilicon gate electrode 106. It should be noted that the structure of the present invention is advantageous in the formation of salicided source/drain extensions. For example, when a metal such as nickel, which diffuses in silicon relatively easily, is used to form a nickel salicide layer, lateral diffusion of nickel atoms is stopped by nitride side wall spacers 108 and the nickel atoms therefore do not penetrate into the channel region where they would otherwise adversely affect the electrical characteristics of the MOSFET. It can be seen in Fig. 4, that the thickness of Si 110 and the depth of salicide layer 114 can be varied with the scope of the invention and still benefit from the structure's metal atom diffusion barrier characteristics.

Referring to Fig. 6, in a further alternative embodiment of the present invention, a layer of phosphorous doped Si 111 is epitaxially formed, prior to an in-situ epitaxial formation of boron doped Si 110. Those skilled in the art and having the benefit of this disclosure will appreciate that other n-type dopants may be used in place of phosphorous. Arsenic is an example of an alternative n-type dopant.

Since the doping concentration of the single crystal epitaxial layer is a function of the gas mixture, temperature, and pressure, in an epitaxial reaction chamber, it is possible to first form a highly doped Si layer (or $\text{Si}_{1-x}\text{Ge}_x$, $x=0$ to 0.3) 111 of a first conductivity type (e.g., n-type by doping with phosphorous). Then without exposing the wafer to the atmosphere, changing the gas mixture, temperature, and pressure, such that a highly doped Si layer 110 of a second conductivity type (e.g., p-type by doping with boron) is formed immediately superjacent Si layer 111. In this way, the recesses in substrate 102 are filled with a bi-layer of single crystal silicon (or $\text{Si}_{1-x}\text{Ge}_x$, $x=0$ to 0.3) having a very abrupt junction.

Desirable electrical characteristics may be obtained in this way by having a relatively lightly doped substrate 102 of a first conductivity type, highly doped source/drain terminals 110 of a second conductivity type, and a highly doped region 111 of the first conductivity type disposed between source/drain terminals 110 and lightly doped substrate 102. Due to the nature of the selective deposition process (described above), highly doped regions 110, 111, are not

only highly doped in the source/drain extension regions, but also in the tip-to-gate overlap region. The term tip, is generally used to refer to that portion of the source/drain junction that is subjacent to the gate and adjacent to the channel portion of a FET.

In conjunction with Fig. 7, the operations of fabricating a FET on a wafer in accordance with an illustrative embodiment of the present invention are described. An operation (block 202) is performed wherein a spacer layer is formed over a patterned gate electrode. In an illustrative embodiment of the present invention, the gate electrode is comprised of polysilicon that has previously been deposited over a gate dielectric layer. The gate dielectric is typically oxidized silicon. In the illustrative embodiment having an oxide gate dielectric and a polysilicon gate electrode, the spacer layer is typically silicon nitride. Those skilled in the art and having the benefit of this disclosure will recognize that the invention is not limited to the combination of an oxide dielectric and polysilicon gate electrode. By way of example and not limitation, the gate dielectric layer may consist of an oxide layer and a nitride layer in combination. Similarly, by way of example and not limitation, the gate electrode may be formed from a metal rather than polysilicon.

After the spacer layer has been formed, it is subjected to an anisotropic etch (block 204) in which sidewall spacers are formed. During the anisotropic etch, portions of the spacer layer that are superjacent the top surface the gate electrode and the top surface of the wafer are removed. The remaining portion of the spacer layer disposed along the opposing vertical sidewalls of the gate electrode.

Recesses are formed in the wafer (block 206) at locations where the source/drain terminals of the FET will be located. The recesses are formed by the isotropic etch of the wafer. As is understood in this field, an isotropic etch operation will remove material from the wafer surface both vertically and laterally. The etch chemistry and conditions are preferably chosen such that the etch is highly selective and preferentially etches the wafer rather than the side wall spacers or the gate dielectric layer. In the illustrative embodiment, wherein the wafer is silicon,

the gate dielectric is an oxide of silicon, the gate electrode is polysilicon and the side wall spacers are silicon nitride, a plasma etch with sulfur hexafluoride (SF_6) and helium (He) is used.

After the recesses are formed, the wafer is typically placed in an epitaxial reactor and a first layer of doped crystalline material is formed (block 208). The crystalline material may be, for example, p-type silicon, p-type silicon germanium, n-type silicon, or n-type silicon germanium. Typically, the conductivity type of the first layer matches the conductivity type of that portion of the wafer where the FET is being fabricated. Those skilled in the art will recognize that various portions of the wafer may be doped and/or counterdoped so as to form wells within which FETs may be formed. For example, n-channel FETs (NFETs) are formed within a p-type region of the wafer, whereas p-channel FETs (PFETs) are formed within an n-type region of the wafer.

After the first layer is formed, a second layer of doped crystalline material is formed (block 210). The second layer is typically formed without exposing the first layer to the atmosphere. That is, the second layer and first layer are formed in a continuous in-situ operation, in the same reaction chamber simply by changing the gas mixture, temperature, and pressure in the epitaxial reactor. The crystalline material may be, for example, p-type silicon, p-type silicon germanium, n-type silicon, or n-type silicon germanium. Typically, the conductivity type of the second layer is chosen to be opposite that of the first layer. In this way, extremely abrupt junctions can be obtained.

For example, a gate structure of a PFET is formed in a region of a n-type portion of a silicon wafer, and after the source/drain recesses are formed, a first layer of n-doped (e.g., phosphorous) silicon germanium is formed in the recesses, and then a second layer of p-doped (e.g., boron) silicon germanium is formed over the first layer. Both the first and second layers have doping concentrations that are substantially higher than the doping concentration of the n-type portion of the silicon wafer, which forms the body terminal of the PFET. More particularly, the first and second layer are substantially free of counterdopants, whereas the n-type region of

the wafer typically contains both n-type and p-type dopants. A gate structure may be a gate electrode or a gate electrode and adjacent side wall spacers.

A salicidation operation is typically performed to further reduce the sheet resistivity of the source/drain terminals and gate electrode.

Conclusion

Embodiments of the present invention provide a field effect transistor structure having very short channel length and low source/drain extension resistivity, yet operable to produce high drive currents without suffering from the short channel effects that produce significant levels of off-state current. Further embodiments of the present invention provide methods of manufacturing such a structure.

An advantage of particular embodiments of the present invention is that source/drain terminals can be formed without annealing. By eliminating the high temperature step conventionally required to activate the dopants, thermal diffusion is avoided and the very abrupt junctions are maintained.

An advantage of particular embodiments of the present invention is that the raised junctions formed by back filling, in conjunction with the side wall spacers disposed along opposing vertical walls of the gate electrode, substantially prevent lateral diffusion of metal atoms in the transistor channel region during the salicidation operation.

An advantage of particular embodiments of the present invention is placement of active dopants directly in the tip portion of the source/drain terminals.

An advantage of particular embodiments of the present invention is that a very precise doping profile is achieved.

An advantage of particular embodiments of the present invention is that very shallow, highly doped, source/drain terminals can be formed without ion implantation of the tip portion. In some cases, even a deep source/drain implant, typically used to form portions of source/drain terminals that lie further from the channel region, may be eliminated.

It will be understood by those skilled in the art having the benefit of this disclosure that many design choices are possible within the scope of the present invention. For example, structural parameters, including but not limited to, gate insulator thickness, gate insulator materials, gate electrode thickness, sidewall spacer material, inter-layer dielectric material, isolation trench depth, and S/D and well doping concentrations may all be varied from that shown or described in connection with the illustrative embodiments. Similarly, the operation of forming recesses and back filling with doped crystalline material may be repeated to tailor the shape and doping profile of the source/drain terminals.

It will be understood that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated may be made by those skilled in the art having the benefit of this disclosure without departing from the principles and scope of the invention as expressed in the subjoined Claims.

What is claimed is:

1. A microelectronic structure, comprising:
 - a substrate having a top surface that defines a first plane;
 - a dielectric disposed superjacent the top surface of the substrate;
 - a gate electrode disposed superjacent the dielectric, the gate electrode having first side wall spacers disposed along opposing vertical walls thereof;
 - a source terminal and a drain terminal each disposed, each substantially adjacent one of the first side wall spacers, partially within the substrate and partially above the substrate, the source and drain terminals further having a portion that extends laterally so as to be subjacent at least a portion of the side wall spacers;
 - wherein the source and drain terminals have top surfaces that define a second plane, the second plane being above the first plane, and the source and drain terminals comprise a doped crystalline semiconductor.
2. The structure of Claim 1, further comprising:
 - a body, disposed within the substrate, having a first portion and a second portion;
 - wherein the first portion is of a first conductivity type and a first doping profile, the second portion is of the first conductivity type and a second doping profile, and a transition between the first doping profile and the second doping profile is abrupt.
3. The structure of Claim 2, wherein the first portion includes counterdopants and the second portion is substantially free of counterdopants.

4. The structure of Claim 1, wherein the gate electrode comprises polysilicon disposed over the gate dielectric; and crystalline silicon of a first conductivity type disposed over the polysilicon.
5. The structure of Claim 4, wherein the gate electrode further comprises a crystalline silicon of a second conductivity type.
6. The structure of Claim 1, further comprising second side wall spacers adjacent the first side wall spacers; and metal salicide disposed in an upper portion of the gate electrode and an upper portion of the source/drain terminals.
7. The structure of Claim 6, wherein the source/drain terminals comprise p-type silicon.
8. The structure of Claim 6, wherein the source/drain terminals comprise n-type silicon.
9. The structure of Claim 6, wherein the source/drain terminals comprise p-type silicon germanium.
10. The structure of Claim 6, wherein the source/drain terminals comprise n-type silicon germanium.
11. A method of making a junction, comprising:
 - a) forming a patterned structure on a surface of a substrate, the substrate being of a first conductivity type;
 - b) isotropically etching the substrate such that a recess in the substrate is formed, the recess including a portion that underlies the patterned structure, the recess having a surface; and
 - c) selectively forming a layer of a first material having a second conductivity type in the recess.

12. The method of Claim 11, further comprising, prior to selectively forming the layer of the first material, selectively forming a layer of a second material having the first conductivity type over the surface of the recess.
13. The method of Claim 12, wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon, and the second material comprises doped silicon.
14. The method of Claim 12, wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon germanium, and the second material comprises doped silicon germanium.
15. The method of Claim 14, wherein the second material has a thickness that is less than a thickness of the first material.
16. The method of Claim 15, wherein the first material has a top surface that is above a plane defined by the surface of the substrate.
17. The method of Claim 11, wherein the patterned structure comprises a dielectric layer and a conductive material disposed over the dielectric layer.
18. The method of Claim 11, wherein etching passivates the surface of the recess.
19. The method of Claim 11, wherein etching comprises exposing the substrate to SF_6 and He in an RF plasma etching system.
20. The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material.

21. The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material; and forming the second material comprises epitaxially depositing a layer of crystalline material; wherein the substrate remains unexposed to the atmosphere subsequent to forming the first material and prior to forming the second material.
22. A method of making a transistor, comprising:
- forming a dielectric on a first surface of a wafer;
 - forming a conductive layer overlying the dielectric;
 - patterning the conductive layer and dielectric so as to form a gate structure;
 - forming recesses adjacent and partially subjacent the gate structure; and
 - in a continuous operation, back filling the recesses with doped crystalline material;
- wherein back filling comprises forming crystalline material of at least a first conductivity type.
23. The method of Claim 22, wherein the crystalline material of the first conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.
24. The method of Claim 22, wherein back filling further comprises forming crystalline material of a second conductivity type.
25. The method of Claim 22, wherein the crystalline material of the second conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.
26. The method of Claim 25, wherein back filling comprises a selective deposition.

27. A method of fabricating a FET, comprising:

forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type;

forming first spacers along the sidewalls of the gate electrode;

forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface;

substantially filling the recess with a first layer of doped crystalline material, the first layer having a second conductivity type.

28. The method of Claim 27, further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate.

29. The method of Claim 27, further comprising forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess.

30. The method of Claim 29, wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1.1 cm, an RF power in the range of

approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium.

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Fig. 1

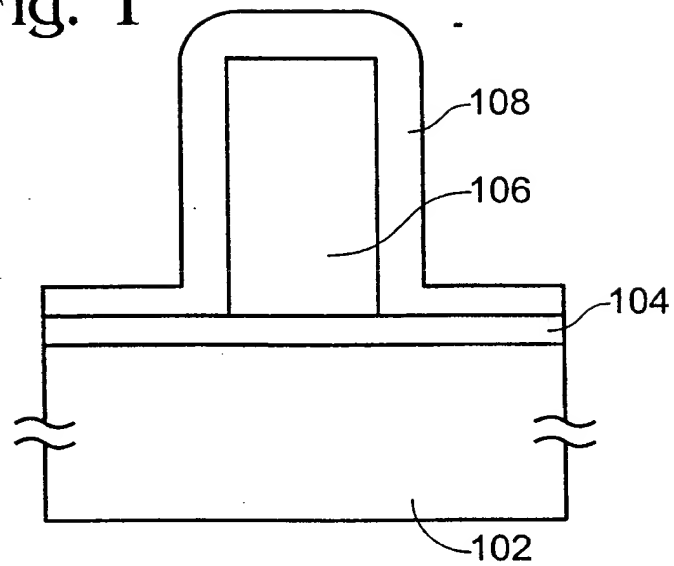
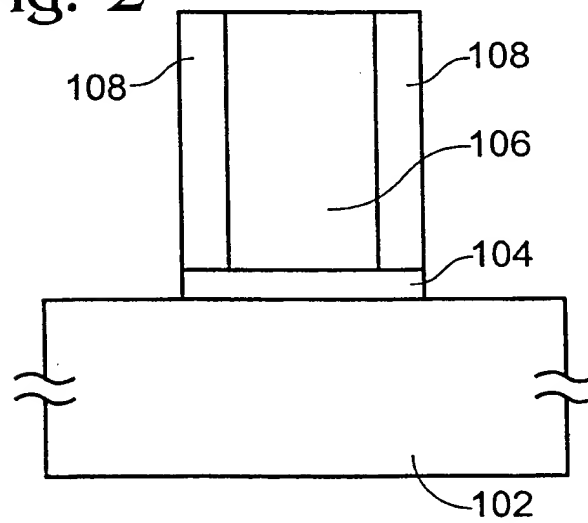


Fig. 2



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Fig. 3

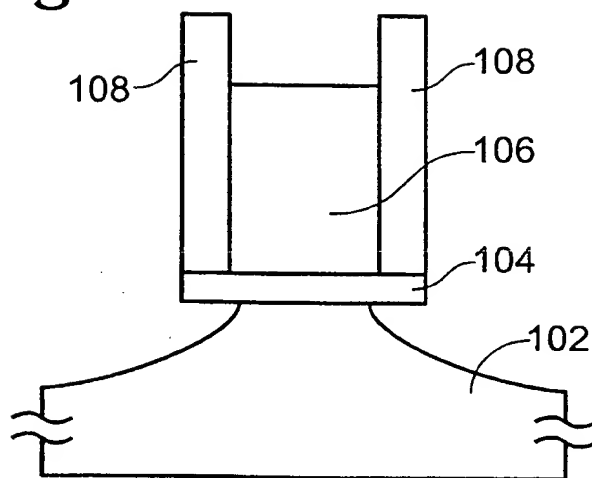
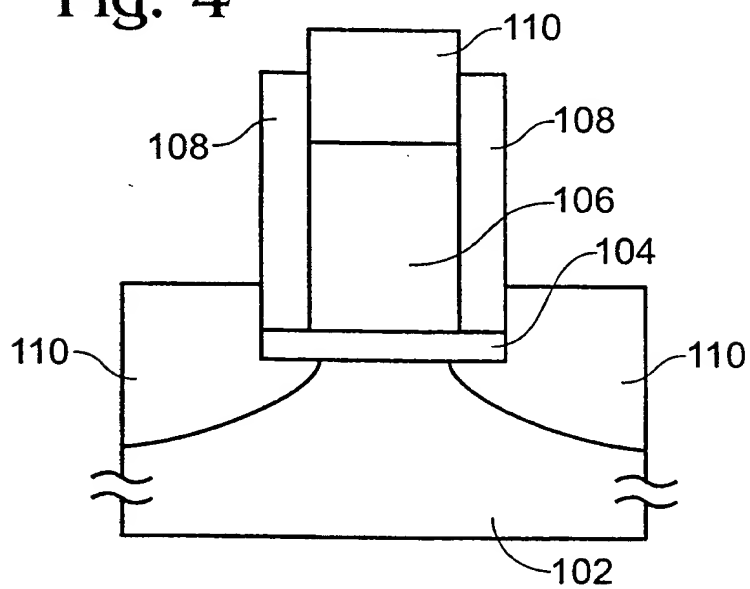


Fig. 4



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Fig. 5

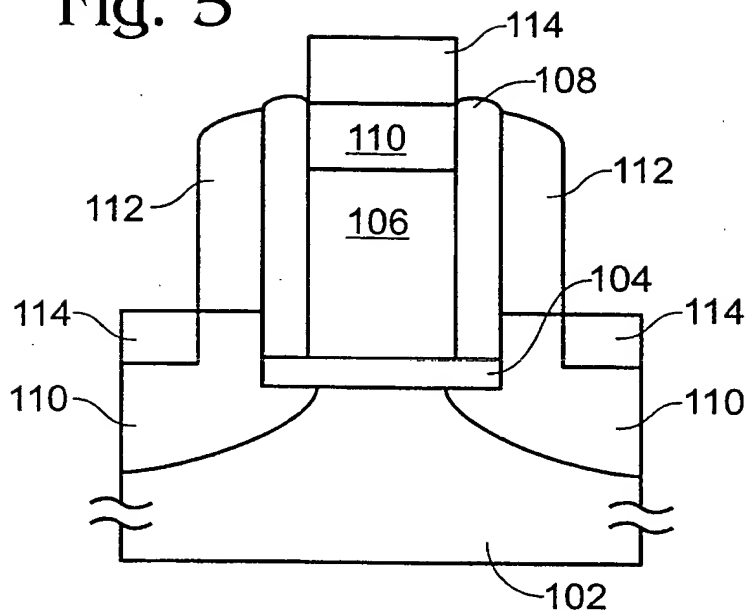
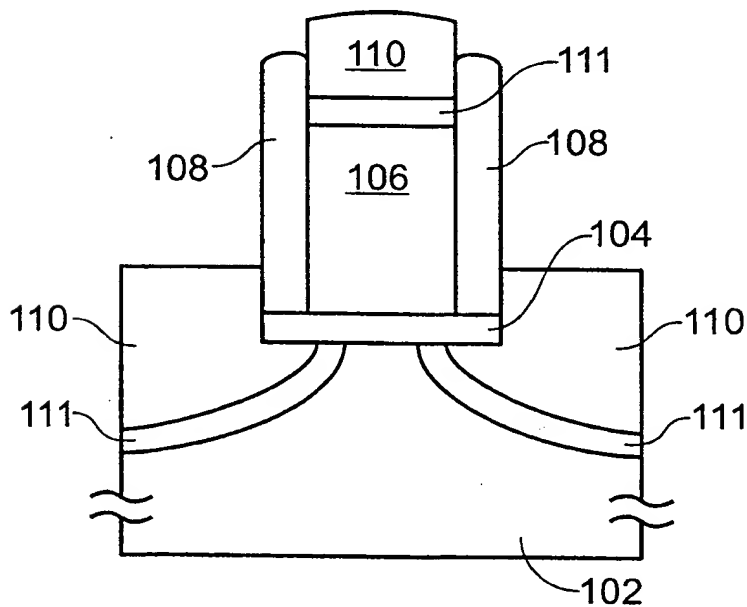


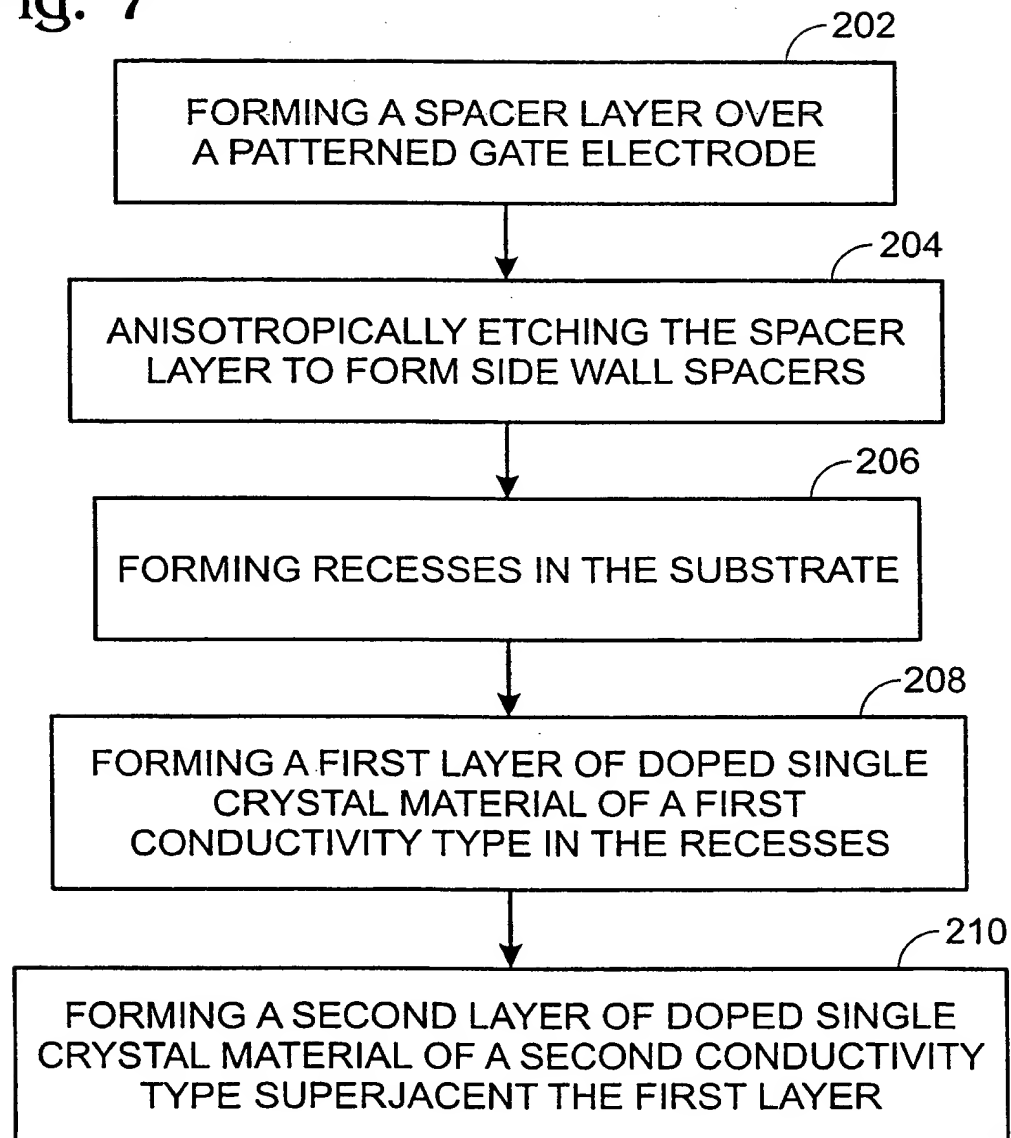
Fig. 6



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Fig. 7

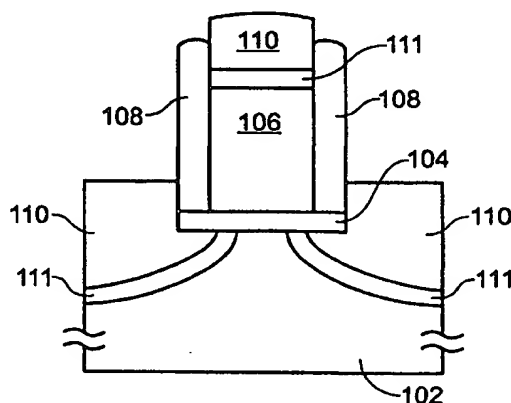


JC08 Rec'd PCT/PTO

10 MAY 2001

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶: H01L 21/336	A1	(11) International Publication Number: WO 00/30169 (43) International Publication Date: 25 May 2000 (25.05.00)
(21) International Application Number: PCT/US99/26224 (22) International Filing Date: 5 November 1999 (05.11.99) (30) Priority Data: 09/191,076 12 November 1998 (12.11.98) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): MURTHY, Anand, S. [IN/US]; Apartment 1304, 1845 N.W. 173rd Avenue, Beaverton, OR 97006 (US). CHAU, Robert, S. [US/US]; 13525 S.W. Harness Lane, Beaverton, OR 97008 (US). MORROW, Patrick [US/US]; 6150 N.W. Simnasho Drive, Portland, OR 97229 (US). JAN, Chia-Hong [-/US]; 395 N.W. 176th Avenue, Portland, OR 97229 (US). PACKAN, Paul [CA/US]; 15025 S.W. Gibraltar Court, Beaverton, OR 97007 (US). (74) Agents: MILLIKEN, Darren, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i>

(54) Title: FIELD EFFECT TRANSISTOR STRUCTURE WITH ABRUPT SOURCE/DRAIN JUNCTIONS**(57) Abstract**

Microelectronic structures embodying the present invention include a field effect transistor (FET) having highly conductive source/drain extensions. Formation of such highly conductive source/drain extensions includes forming a passivated recess which is back filled by epitaxial deposition of doped material to form the source/drain junctions. The recesses include a laterally extending region that underlies a portion of the gate structure. Such a lateral extension may underlie a sidewall spacer (108) adjacent to the vertical sidewalls of the gate electrode (106), or may extend further into the channel portion of a FET such that the lateral recess underlies the gate electrode portion of the gate structure. In one embodiment the recess is back filled by an in-situ epitaxial deposition of a bilayer of oppositely doped material. In this way, a very abrupt junction is achieved that provides a relatively low resistance source/drain extension and further provides good off-state subthreshold leakage characteristics. Alternative embodiments can be implemented with a back filled recess of a single conductivity type.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26224**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) : HO1L 21/336

US CL : 438/300

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/300, 438/299, 438/713, 438/488, 438/481, 438/341, 438/365

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONEElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,300,447 A (Anderson) 05 April 1994, (05/04/94), fig. 1b	1, 11, 22
Y	US 4,870,029 A (Easter et al.) 26 September 1989, (26/09/89), figs. 3-6, cols. 2-4	11
X	US 5,504,018 A (Sato) 2 April 1996, (02/04/96), cols. 10-13	7, 9-10, 14-15, 25
X	S.Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, V1-Process Technology, pp 173-174, 545-547	11, 30

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
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Date of the actual completion of the international search

14 JANUARY 2000

Date of mailing of the international search report

10 FEB 2000

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Commissioner of Patents and Trademarks
Box PCT
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Facsimile No. (703) 305-3230

Authorized officer

CHANDRA CHAUDHARI

Telephone No. (703) 308-0000

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26224

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,714,685 A (Schubert) 22 December 1987, (22/12/87), figs. 1-19, cols 3-8	1-6, 8, 11-13, 16-18, 20, 22-24, 26-29

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
MICHAEL J. MALLIE
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES, CA

PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing
(day/month/year)

22 MAY 2001

Applicant's or agent's file reference

42390.P6624PCT

IMPORTANT NOTIFICATION

International application No.

International filing date (day/month/year)

Priority date (day/month/year)

PCT/US99/26224

05 November 1999 (05.11.1999)

12 November 1998 (12.11.1998)

Applicant

INTEL CORPORATION

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.
2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.
3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.
4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US

Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703)305-3230

Authorized officer

Wael Fahmy

Telephone No. 703-308-1778



I. Basis of the report

1. With regard to the elements of the international application:*

- ☒ the international application as originally filed.
- ☒ the description:
pages 1-15 as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.
- ☒ the claims:
pages 16-21 as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.
- ☒ the drawings:
pages 1-4 as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.
- ☐ the sequence listing part of the description:
pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language _____ which is:

- ☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in printed form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

- ☒ the description, pages NONE
- ☒ the claims, Nos. NONE
- ☒ the drawings, sheets/fig NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).

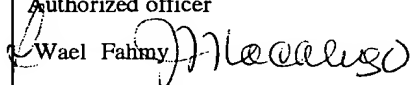
** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 42390.P6624PCT	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/US99/26224	International filing date (<i>day/month/year</i>) 05 November 1999 (05.11.1999)	Priority date (<i>day/month/year</i>) 12 November 1998 (12.11.1998)
International Patent Classification (IPC) or national classification and IPC IPC(7): HO1L 21/336 and US Cl.: 438/300		
Applicant INTEL CORPORATION		
<p>1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.</p> <p>2. This REPORT consists of a total of <u>5</u> sheets, including this cover sheet.</p> <p><input type="checkbox"/> This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).</p> <p>These annexes consist of a total of <u>0</u> sheets.</p>		
<p>3. This report contains indications relating to the following items:</p> <ul style="list-style-type: none"> I <input checked="" type="checkbox"/> Basis of the report II <input type="checkbox"/> Priority III <input type="checkbox"/> Non-establishment of report with regard to novelty, inventive step and industrial applicability IV <input type="checkbox"/> Lack of unity of invention V <input checked="" type="checkbox"/> Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement VI <input type="checkbox"/> Certain documents cited VII <input type="checkbox"/> Certain defects in the international application VIII <input type="checkbox"/> Certain observations on the international application 		
Date of submission of the demand 31 May 2000 (31.05.2000)	Date of completion of this report 15 May 2001 (15.05.2001)	
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer <div style="text-align: center;">  Wael Fahmy </div> Telephone No. 703-308-1778	

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**1. STATEMENT**

Novelty (N)	Claims <u>1-10, 12-21, 23-26, 28-30</u>	YES
	Claims <u>11, 22 and 27</u>	NO
Inventive Step (IS)	Claims <u>NONE</u>	YES
	Claims <u>1-30</u>	NO
Industrial Applicability (IA)	Claims <u>1-30</u>	YES
	Claims <u>NONE</u>	NO

2. CITATIONS AND EXPLANATIONS (Rule 70.7)

Please See Continuation Sheet

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

C ntinuation of Section I. Basis of the opinion, Item 5
NONE**V. 2. Citations and Explanations:**

Claim no(s). 11, 22, and 27 lack novelty under PCT Article 33(2) as being anticipated by Y.Mitani et al. (IEEE).

Y.Mitani et al. in figs. 1-7 and related text discloses the claimed invention including forming a dielectric on a first surface of a wafer (fig. 2); forming a conductive layer overlying the dielectric (fig. 2, gate); patterning the conductive layer so as to form the gate (fig. 2); forming sidewall spacers (fig. 2); forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface (fig. 2). The term gate is interpreted as including the spacers. See *In re Zletz*, 13 USPQ2d 1320 (Fed. Cir. 1989)(Claims are given their broadest possible interpretation during PTO prosecution).

Substantially filling the recess with a first layer of doped crystalline material. (fig. 2, col. 1-2, pp. 176).

Claim no(s). 11-30 lack an inventive step under PCT Article 33(3) as being obvious over Y.Mitani (IEEE) in view of Takashi Uchino (IEEE) in view of Wolf et al..

Y.Mitani discloses supra, however lacks anticipation for forming doped SiGe.

Takashi Uchino (IEEE) discloses depositing doped SiGe and doped Si growth techniques as is conventional in the art to form source/drain regions. Uchino teaches the use of SiGe and Si as art recognized equivalents (abs). Therefore, it would have been obvious to one of ordinary skill in the art to use doped SiGe epi instead of the doped Si of Y.Mitani because they are art recognized equivalents as disclosed by Uchino.

Y.Mitani discloses supra, and isotropic etching however lacks anticipation for the claimed etching conditions.

Wolf discloses (pp. 542-555) conventional plasma etching techniques using SF₆ in which an RF diode configuration is normally used with conventional parallel plate reaction chambers (pp. 171-174). It would have been obvious for one of ordinary skill in the art to employ the process of Wolf for its disclosed intended purpose to achieve the etching step of Y.Mitani.

Examiner takes official notice that the selection of He gas was known at the time of the applicants invention as a carrier gas. It would be obvious to employ the known prior art process for it's known intended purpose to achieve the plasma etching step of combination.

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

The selection of the operating conditions (e.g., plate separation, pressure, and power) would amount to routine optimization within the teachings of the reference are known to be result effective variables. Therefore they are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Claim no(s). 1-10 lack an inventive step under PCT Article 33(3) as being obvious over Y. Mitani (IEEE) in view of Takashi Uchino (IEEE).

Y. Mitani discloses in figures 1-7 and related text a microelectronic structure comprising a substrate having a top surface that defines a first plane (fig. 2); a dielectric disposed superjacent the top surface of the substrate (fig. 2); a gate electrode disposed superjacent the dielectric, the gate electrode having first side wall spacers disposed along opposing vertical walls thereof (fig. 2)

A source terminal and a drain terminal each disposed, each substantially adjacent one of the first side wall spacers, partially within the substrate and partially above the substrate (fig. 2, e.g., doped si) the source/drain terminals further having a portion that extends laterally so as to be subjacent at least a portion of the of the side wall spacers (fig. 2);

wherein the source/drain terminals have top surfaces that define a second plane, the second plane being above the first plane (fig. 2), and the source and drain terminals comprised doped crystalline material (fig. 2).

The selection of the dopant conductivity is notoriously obvious in the art. (e.g., p-type, n-type)

Uchino teaches the use of poly-si gates or NMOS or PMOS devices. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Uchino for their disclosed intended purposes of forming gates.

Claims 1-30 meets have industrial applicability set out in PCT Article 33(4), because the invention can be used in the semiconductor industry.

----- NEW CITATIONS -----

Y. Mitani et al., Buried Source and Drain (BSD) Structure for Ultra-shallow Junction Using Selective Deposition of Highly Doped Amorphous Silicon, (IEEE), 1996, pgs. 176-177

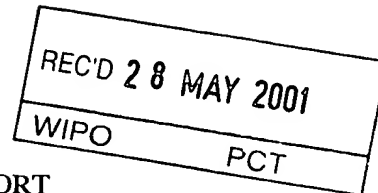
Takashi Uchino, et al., A raised Source/Drain Technology Using In-Situ P-doped SiGe and B-Doped Si for 0.1 um CMOS ULSIs, 1997, (IEEE), pgs. 479-482

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)



14

Applicant's or agent's file reference 42390.P6624PCT		FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/US99/26224	International filing date (day/month/year) 05 November 1999 (05.11.1999)	Priority date (day/month/year) 12 November 1998 (12.11.1998)	
International Patent Classification (IPC) or national classification and IPC IPC(7): HO1L 21/336 and US Cl.: 438/300			
Applicant INTEL CORPORATION			
<p>1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.</p> <p>2. This REPORT consists of a total of <u>5</u> sheets, including this cover sheet.</p> <p><input type="checkbox"/> This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).</p> <p>These annexes consist of a total of <u>0</u> sheets.</p> <p>3. This report contains indications relating to the following items:</p> <p>I <input checked="" type="checkbox"/> Basis of the report</p> <p>II <input type="checkbox"/> Priority</p> <p>III <input type="checkbox"/> Non-establishment of report with regard to novelty, inventive step and industrial applicability</p> <p>IV <input type="checkbox"/> Lack of unity of invention</p> <p>V <input checked="" type="checkbox"/> Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</p> <p>VI <input type="checkbox"/> Certain documents cited</p> <p>VII <input type="checkbox"/> Certain defects in the international application</p> <p>VIII <input type="checkbox"/> Certain observations on the international application</p>			
Date of submission of the demand 31 May 2000 (31.05.2000)		Date of completion of this report 15 May 2001 (15.05.2001)	
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230		Authorized officer Wael Fahmy <i>Wael Fahmy</i> Telephone No. 703-308-1778	

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.

PCT/US99/26224

I. Basis of the report

1. With regard to the elements of the international application:*

- ☒ the international application as originally filed.
- ☒ the description:
 pages 1-15 as originally filed
 pages NONE, filed with the demand
 pages NONE, filed with the letter of _____
- ☒ the claims:
 pages 16-21 as originally filed
 pages NONE, as amended (together with any statement) under Article 19
 pages NONE, filed with the demand
 pages NONE, filed with the letter of _____
- ☒ the drawings:
 pages 1-4 as originally filed
 pages NONE, filed with the demand
 pages NONE, filed with the letter of _____
- ☐ the sequence listing part of the description:
 pages _____ as originally filed
 pages _____, filed with the demand
 pages _____, filed with the letter of _____

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language _____ which is:

- ☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in printed form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

- ☒ the description, pages NONE
- ☒ the claims, Nos. NONE
- ☒ the drawings, sheets/fig NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).

** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.

PCT/US99/26224

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**1. STATEMENT**

Novelty (N)

Claims 1-10, 12-21, 23-26, 28-30 YESClaims 11, 22 and 27 NO

Inventive Step (IS)

Claims NONE YESClaims 1-30 NO

Industrial Applicability (IA)

Claims 1-30 YESClaims NONE NO**2. CITATIONS AND EXPLANATIONS (Rule 70.7)**

Please See Continuation Sheet

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

C ntinuation of Section I. Basis of the opinion, Item 5

NONE

V. 2. Citations and Explanations:

Claim no(s). 11, 22, and 27 lack novelty under PCT Article 33(2) as being anticipated by Y.Mitani et al. (IEEE).

Y.Mitani et al. in figs. 1-7 and related text discloses the claimed invention including forming a dielectric on a first surface of a wafer (fig. 2); forming a conductive layer overlying the dielectric (fig. 2, gate); patterning the conductive layer so as to form the gate (fig. 2); forming sidewall spacers (fig. 2); forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface (fig. 2). The term gate is interpreted as including the spacers. See *In re Zletz*, 13 USPQ2d 1320 (Fed. Cir. 1989)(Claims are given their broadest possible interpretation during PTO prosecution).

Substantially filling the recess with a first layer of doped crystalline material. (fig. 2, col. 1-2, pp. 176).

Claim no(s). 11-30 lack an inventive step under PCT Article 33(3) as being obvious over Y.Mitani (IEEE) in view of Takashi Uchino (IEEE).

Y.Mitani discloses supra, however lacks anticipation for forming doped SiGe.

Takashi Uchino (IEEE) discloses depositing doped SiGe and doped Si growth techniques as is conventional in the art to form source/drain regions. Uchino teaches the use of SiGe and Si as art recognized equivalents (abs). Therefore, it would have been obvious to one of ordinary skill in the art to use doped SiGe epi instead of the doped Si of Y.Mitani because they are art recognized equivalents as disclosed by Uchino.

Y.Mitani discloses supra, and isotropic etching however lacks anticipation for the claimed etching conditions.

Wolf discloses (pp. 542-555) conventional plasma etching techniques using SF₆ in which an RF diode configuration is normally used with conventional parallel plate reaction chambers (pp. 171-174). It would have been obvious for one of ordinary skill in the art to employ the process of Wolf for its disclosed intended purpose to achieve the etching step of Y.Mitani.

Examiner takes official notice that the selection of He gas was known at the time of the applicants invention as a carrier gas. It would be obvious to employ the known prior art process for it's known intended purpose to achieve the plasma etching step of combination.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/26224

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

The selection of the operating conditions (e.g., plate separation, pressure, and power) would amount to routine optimization within the teaches of the reference are known to be result effective variables. Therefore they are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Claim no(s). 1-10 lack an inventive step under PCT Article 33(3) as being obvious over Y.Mitani (IEEE) in view of Takashi Uchino (IEEE).

Y.Mitani discloses in figures 1-7 and related text a microelectronic structure comprising a substrate having a top surface that defines a first plane (fig. 2); a dielectric disposed superjacent the top surface of the substrate (fig. 2); a gate electrode disposed superjacent the dielectric, the gate electrode having first side wall spacers disposed along opposing vertical walls thereof (fig. 2)

A source terminal and a drain terminal each disposed, each substantially adjacent one of the first side wall spacers, partially within the substrate and partially above the substrate (fig. 2, e.g., doped si) the source/drain terminals further having a portion that extends laterally so as to be subjacent at least a portion of the of the side wall spacers (fig. 2);

wherein the source/drain terminals have top surfaces that define a second plane, the second plane being above the first plain (fig. 2), and the source and drain terminals comprised doped crystalline material (fig. 2).

The selection of the dopant conductivity is notoriously obvious in the art. (e.g., p-type, n-type)

Uchino teaches the use of poly-si gates or NMOS or PMOS devices. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Uchino for their disclosed intended purposes of forming gates.

Claims 1-30 meets have industrial applicability set out in PCT Article 33(4), because the invention can be used in the semiconductor industry.

NEW CITATIONS

Y.Mitani et al., Buried Source and Drain (BSD) Structure for Ultra-shallow Junction Using Selective Deposition of Highly Doped Amorphous Silicon, (IEEE), 1996, pgs. 176-177

Takashi Uchino, et al., A raised Source/Drain Technology Using In-Situ P-doped SiGe and B-Doped Si for 0.1 um CMOS ULSIs, 1997, (IEEE), pgs. 479-482

PATENT COOPERATION TREATY

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

From the INTERNATIONAL BUREAU

To:

Assistant Commissioner for Patents
United States Patent and Trademark
Office
Box PCT
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in its capacity as elected Office

Date of mailing (day/month/year)
28 August 2000 (28.08.00)

International application No.
PCT/US99/26224

Applicant's or agent's file reference
42390.P6624

International filing date (day/month/year)
05 November 1999 (05.11.99)

Priority date (day/month/year)
12 November 1998 (12.11.98)

Applicant

MURTHY, Anand, S. et al

1. The designated Office is hereby notified of its election made:

☒ in the demand filed with the International Preliminary Examining Authority on:

31 May 2000 (31.05.00)

☐ in a notice effecting later election filed with the International Bureau on:

2. The election ☒ was

☐ was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

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for the VLSI Era

Volume 1—Process Technology

S. Wolf and R.N. Tauber

approximately equal. Rf tuning networks of PECVD systems therefore usually employ an inductor which shunts the powered electrode to ground to establish this condition. Grounding prevents the powered electrode from developing a larger self-bias, thereby maintaining approximately equal average potentials between the plasma and the powered and grounded electrodes. The walls of parallel plate reactors are made of either quartz, ceramic, or aluminum oxide coated steel, in order to place them at a floating potential with respect to the plasma. This minimizes wall bombardment and sputtering, which reduces contamination of the growing films. (Note that the quartz tube of tube PECVD reactors is an insulator, and thus does not require such coating).

Parallel Plate PECVD Reactors

The radial parallel plate reactor was developed by Reinberg⁵² in the early 1970's, and the first commercial model was offered in 1976. A schematic of this reactor type is shown in Fig. 8a. The reaction chamber is a short, vertically oriented cylinder, typically constructed of stainless steel. The rf power (at frequencies of 450 kHz-13.5 MHz) which establishes the plasma is applied to the upper electrode, and the wafers reside on the bottom grounded electrode, which can be rotated for improved uniformity, and be heated up to 400°C. The electrode spacing is typically 5 to 10 cm, and such systems operate in the pressure range of 0.1-5 torr. The reactants are introduced either through the center and removed from the periphery (Reinberg design), or from the periphery and removed from the center. Despite depletion effects, uniform deposition can be achieved by correctly balancing the plasma density and gas flows. Parallel plate systems, however, suffer from low throughput for large diameter wafers. In addition, particulates flaking off walls or the upper electrode, can fall onto the horizontally positioned wafers.

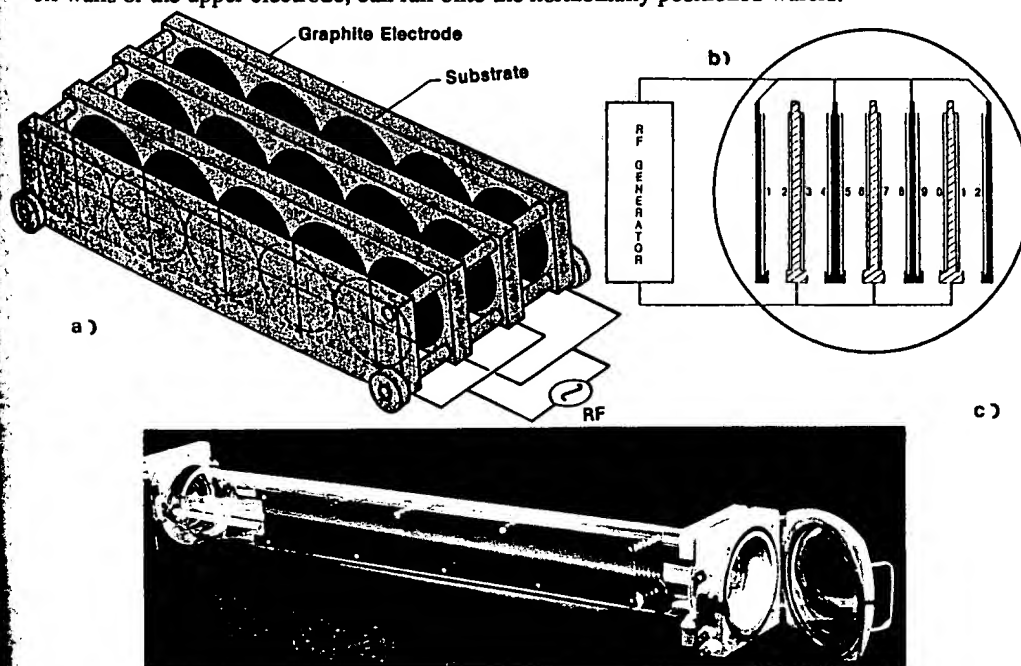


Fig. 9 (a) Long, multiple plate reactor generates plasma between the wafers facing each other on graphite electrodes¹⁴. (b) Cross section of electrode assembly and wafers shown in (a). Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet. (c) Photograph of tubular PECVD reactor. Courtesy of Pacific Western Systems.

Horizontal Tube PECVD Reactors

In 1979 a new PECVD reactor design, the *horizontal tube* reactor, was introduced. This design allows PECVD reactor throughputs to be greatly increased. The reactor resembles a "hot wall" LPCVD system. It consists of a long horizontal quartz tube that is radiantly heated. Gas is fed into one end, and flows linearly to the other. Special long rectangular graphite plates (Fig. 9) serve both as the electrodes that are needed to establish a plasma, and as holders of the wafers (the electrode configuration is also designed to provide a uniform plasma environment for each wafer, to ensure uniformity of deposition). These vertically-oriented graphite electrodes are stacked parallel to one another, side-by-side, with alternating plates serving as power and ground for the rf voltage. A plasma is formed in the space between each pair of plates.

The use of several long slabs allows an increased number of wafers (up to 120 100mm wafers) to be loaded into the reactor at one time. Most systems consist of two stacked deposition tubes. In addition, since the wafers are held vertically, most particulates do not fall on the wafer surfaces. The entire graphite assembly is withdrawn from the reactor for wafer loading, and then reinserted for processing. Care must be exercised, however, to prevent particulate contamination when loading and unloading wafers from these systems.

Tubular PECVD reactors, like horizontal tube LPCVD reactors, suffer from a depletion effect, but resultant deposition nonuniformities can be minimized by temperature ramping. Another technique used to combat depletion effect nonuniformities is to pulse the plasma, so that during the off phase of the duty cycle, fresh reactant gases fill the tube and replace depleted gases.

Single Wafer PECVD Reactors

The most recently introduced PECVD reactor is the single-wafer design (Fig. 8b). The reactor is load locked, offers cassette-to-cassette operation, provides rapid radiant heating of each wafer, and allows *in situ* monitoring of the film deposition. Wafers ≥ 200 mm can be accommodated. Little direct information on the operational characteristics of such reactors was available at the time of publication, but such reactors are clearly being designed to allow fabrication of large wafers in low-particulate, automated environments.

Photon-Induced Chemical Vapor Deposition

A final CVD method, which may fill the need for an extremely low temperature deposition process without the film composition problems of PECVD, is PHoton-induced Chemical Vapor Deposition (PHCVD). PHCVD uses high-energy, high-intensity photons to either heat the substrate surface, or to dissociate and excite reactant species in the gas phase. In the case of substrate surface heating, the reactant gases are transparent to the photons, and the potential for gas phase reactions is completely eliminated. In the case of reactant gas excitation, the energy of the photons can be chosen for efficient transfer of energy to either the reactant molecules themselves, or to a catalytic intermediary, such as mercury vapor. This technique enables deposition at extremely low (i.e. room) substrate temperatures. PHCVD films show good step coverage, but may suffer from low density and molecular contamination as a result of the low deposition temperature.

There are two classes of PHCVD reactors, depending on energy source: a) UV lamp; and b) laser. *UV lamp reactors*¹⁵ generally use mercury vapor for energy transfer between photons and the reactant gases. UV radiation at 2537Å is efficiently absorbed by mercury atoms, which then transfer energy to the reactant species. Deposition rates for UV PHCVD reactors are typically much slower than in other low temperature techniques. *Laser PHCVD reactors*¹⁶ offer the advantages of *frequency tunability* and a high intensity light source. Tunability is useful in that

reactions and ion-atom

reactions that can take place.

The properties listed above, impart glow discharges with unique and useful capabilities. The first ionization potential of most gas atoms and molecules is ≥ 8 eV. Since the energies of the electrons have a distribution whose average is between 1-10 eV, some of these electrons will be energetic enough to cause such ionization. Collisions of these energetic electrons with neutral etch gas molecules (Table 1), in fact, are primarily responsible for the production of the reactive species in a plasma (*electron-impact reactions*). These reactive species, however, can also react with themselves in the plasma (*inelastic collisions among heavy particles*, Table 1), and alter the overall plasma chemistry.

The most abundant ionic specie found in CF_4 plasmas is CF_3^+ , and such ions are formed by the electron-impact reaction³: $e + \text{CF}_4 \Rightarrow \text{CF}_3^+ + \text{F} + 2e$. Other ionization reactions also occur, but the products of these reactions are found in less abundance than CF_3^+ ions, because the probability that such reactions occur is smaller, and their products also react with CF_4 , while CF_3^+ ions do not. In addition to CF_4 molecules, ionic species, and electrons, there are a large number of radicals that are formed. A radical is an atom, or collection of atoms, which is electrically neutral, but which also exists in a state of incomplete chemical bonding, making it very reactive. Some examples of radicals include F, Cl, O, H, and CF_x , where $x = 1, 2$, or 3 . In CF_4 plasmas, the most abundant radicals are CF_3 and F, formed by the reaction: $e + \text{CF}_4 \Rightarrow \text{CF}_3 + \text{F} + e$. In general, radicals are thought to exist in plasmas in much higher concentrations than ions, because they are generated at a faster rate, and they survive longer than ions in the plasma. This view is substantiated by measurements of radical concentrations in plasmas, but in fact, only a few such measurements have been reported. One measurement determined that the F atom pressure was 20 percent of the total gas pressure in the system⁴. To summarize, the gas in an etch chamber when plasma etching is underway, generally consists of the following species⁵ (in order of decreasing concentration, and estimated concentration ranges): a) etch gas molecules (70-98% of the total species in the chamber); b) etch-product molecules (2-20%); c) radicals 0.1-20%; charged species, including positive ions, electrons, and negative ions (0.001-0.01%).

The radicals, in fact, are responsible for most of the actual chemical etching phenomena that occur at the surface of the material being etched (except for the etching of Al, which is apparently etched by molecular Cl_2). As will be described later, the ionic species are believed primarily to enhance the etching that occurs, by causing events that are not in themselves chemical reactions. Thus, the term *reactive ion etching*, that is commonly used to denote processes in which plasma etching is accompanied by ionic bombardment, is actually somewhat of a misnomer. Since the etching by the reactive radicals is principally enhanced by the ionic bombardment, these processes would more aptly be described as *ion-assisted etching processes*.

Electrical Aspects of Glow Discharges

It is important to have some information about the electrical potential distribution in systems containing glow discharges. In Chap. 10, details about this subject were given for both dc and rf diode glow discharges, and the information was used to explain how glow discharge sputtering occurs. In plasma etching systems, high frequency (13.5 MHz) rf diode configurations are primarily used, and readers are directed to Chap. 10 for more general information on rf glow discharges. In plasma etching systems, knowledge about the potential distribution is useful because the energy with which particles impinge on the etched surface depends on the potential distribution. In addition, the plasma potential determines the energy with which ions strike other surfaces in the chamber, and high energy bombardment of these surfaces can cause sputtering and consequent redeposition of the sputtered material (as contamination on the wafers).

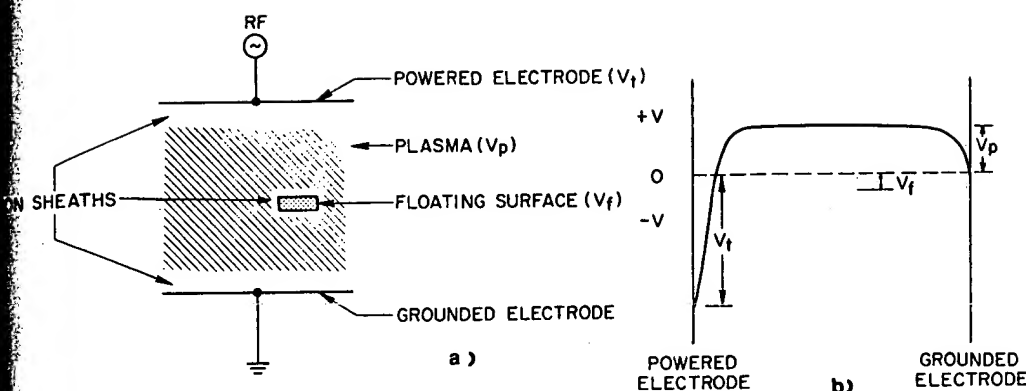


Fig. 4 (a) Schematic view of an rf glow discharge. (b) Potential distribution in a parallel plate plasma etcher with a grounded surface area larger than the powered electrode area.

As shown in Fig. 4 the potential of the plasma is positive relative to that of the grounded electrode (which is usually connected electrically to the chamber walls, grounding them as well), and the powered electrode develops a negative dc self-bias voltage relative to ground, as described in Chap. 10⁶. The magnitude of the self-bias voltage depends on the amplitude of the rf signal applied to the electrodes. As also noted in Chap. 10, if the electrodes of the rf plasma system are of comparable area, the potential difference across the dark space of both electrodes will be equal. Since the powered electrode develops a negative dc self-bias voltage, in order for a potential difference of equal magnitude to exist across the dark space of the grounded electrode, the plasma must assume a positive potential of comparable magnitude. Thus, even if wafers are placed on the grounded electrode of such systems, they will be subjected to substantial energetic ion bombardment. In systems in which the area of the powered electrode is much smaller than that of the grounded electrode, smaller potential differences exist between the plasma and the grounded electrode, and thus grounded surfaces are subjected to less energetic bombardment.

If a 13.56 MHz frequency is used for the applied rf power, this frequency is high enough so that the ions require several rf cycles to traverse the dark space between the bulk plasma region and the wafer surface. Some investigation of systems using lower frequency power has also been conducted (100-450 kHz). Under such circumstances, the ions can cross the dark space in a relatively small fraction of an rf cycle. This can enable ions to strike the surface with greater energies than in the high frequency case, a condition that can be useful in some applications.

Heterogeneous (Surface) Reaction Considerations

The reactive etch species that undergo chemical reactions at the surface that result in etching, and the ionic species that bombard the surface to enhance such etching are produced in the plasma. The events that take place at the surface are interactions between the gas phase species and the solid material to produce etching. The issues related to the mechanisms that occur on the surface include³²: a) the sticking probabilities of radicals and ions; b) chemical recombination processes that form films, cause species to be adsorbed, or lead to other gas phase species; c) reaction paths which are followed, from adsorption to the eventual formation of volatile products; d) desorption of species from the surface; e) effect of ion and electron fluxes on the surface; and f) the synergistic effects on the surface of multiple species bombardment (i.e. by ions, electrons, and photons). As shown in Fig. 5, some of the parameters that impact heterogeneous reactions⁸, include the surface temperature, the surface electrical potential, the nature of the surface, and

Table 2 EXAMPLES OF SOLID-GAS SYSTEMS USED IN SMA ETCHING

SOLID	ETCH GAS	ETCH PRODUCT
Si, SiO ₂ , Si ₃ N ₄	CF ₄ , SF ₆ , NF ₃	SiF ₄
Si	Cl ₂ , CCl ₂ F ₂	SiCl ₂ , SiCl ₄
Al	BCl ₃ , CCl ₄ , SiCl ₄ , Cl ₂	AlCl ₃ , Al ₂ Cl ₆
Organic Solids	O ₂	CO, CO ₂ , H ₂ O
	O ₂ + CF ₄	CO, CO ₂ , HF
Refractory Metals (W, Ta, Mo...)	CF ₄	WF ₆ , ...

geometrical aspects of the surface (e.g. the angle of incidence of impinging ions depends upon whether they are striking the bottom, or the sidewall of an etched feature).

The gases adopted for plasma etching processes have been selected on the basis of their ability to form reactive species in a plasma, which then react with the surface materials being etched and lead to volatile products. Table 2 lists the gas-solid systems for various solids to be etched in VLSI fabrication, together with their resultant etch products.

Parameter Control in Plasma Processes

One of the more challenging aspects of implementing a useful and reproducible etch process

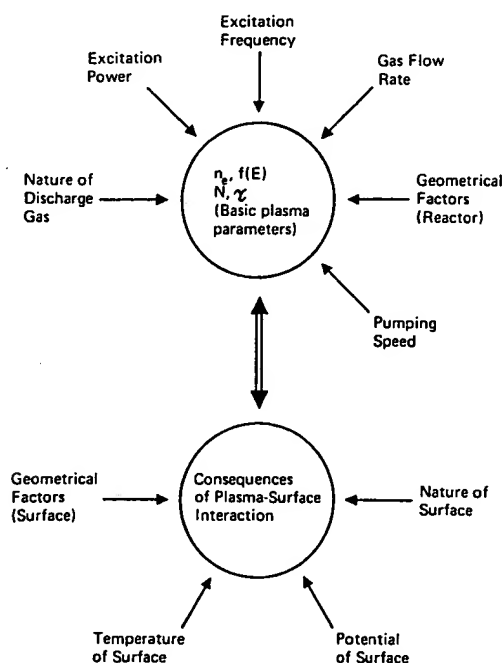


Fig. 5 Representation of the parameter problem in plasma etching systems (n_e is the electron density, $f(E)$ is the electron energy distribution function, N is the gas density, and τ is the residence time⁸. Reprinted with permission of Springer-Verlag Publishing Company.

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Fig. 6 The
temperature

involves the control of the large number of parameters that affect the process. Figure 5 illustrates some of the parameters that impact the gas-phase interactions, as well as the surface-plasma interactions. Although many macroscopic parameters can be controlled, such as the type of feed gas, power, and pressure, the precise effect of making any changes in these parameters is usually not well understood. In fact, a change in a single macroscopic parameter typically alters two or more basic *plasma* parameters, and possibly one or more of the surface parameters, such as temperature or electrical potential. This makes process development in plasma systems a challenge, and the use of factorial experimental design techniques for such tasks very useful⁹ (see Chap. 18). In the introduction to the section on *Dry-Etch System Configurations*, a discussion is presented on how gas flow, pumping speed, and pressure are interrelated, and how this interrelationship is used to control pressure.

ETCHING SILICON and SILICON DIOXIDE in FLUOROCARBON-CONTAINING PLASMAS

The etching of silicon and SiO_2 in fluorocarbon plasmas is described in this section in substantial detail. This is done because these etching processes are very important in silicon VLSI fabrication. In addition, when the mechanisms of plasma etching were being first studied, the etching of silicon and SiO_2 in plasmas containing CF_4 , mixtures of $\text{CF}_4 + \text{O}_2$, and mixtures of $\text{CF}_4 + \text{H}_2$, yielded important data about many of the fundamental mechanisms that are operative in plasma etching, as well as information about the specific materials system under investigation. The conclusions from these studies led to the development of two models for organizing chemical and physical information on plasma etching. These models are the *fluorine-to-carbon ratio model* (or *F/C model*)¹⁰, and the *etchant-unsaturate model*¹¹. Since the models are conceptually similar, although they emphasize different aspects of plasma etching, we describe only the F/C model. Details of the etchant-unsaturate model are given in Ref. 25.

We begin the discussion by considering several basic phenomena related to plasma etching processes. First, it is known that in the absence of a glow discharge, the gases commonly used in plasma etching do not react with the surfaces to be etched. For example, CF_4 does not etch silicon without a discharge. This is due to the fact that CF_4 does not chemisorb on Si, and thus

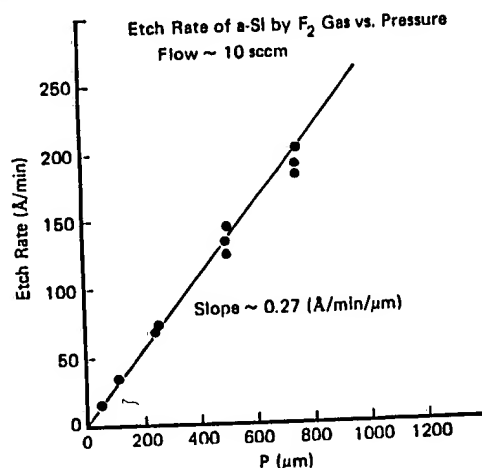


Fig. 6 The fluorine pressure dependence of the etch rate of amorphous silicon at room temperature¹². Reprinted with permission of the publisher, the Electrochemical Society.

